

4 Hardware Characteristics

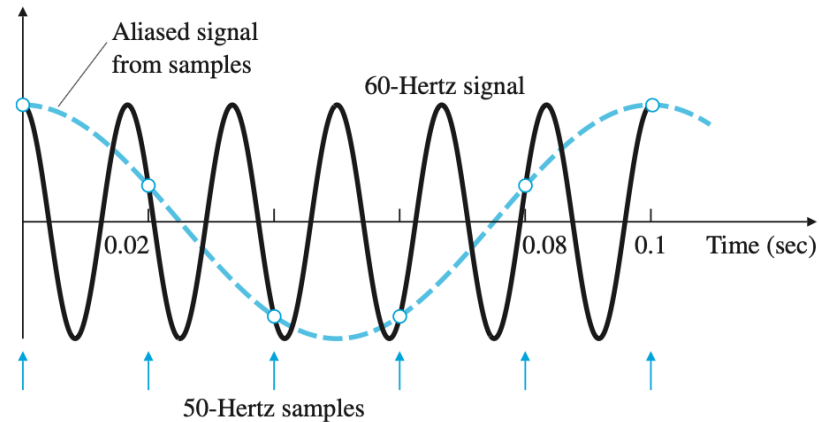
- Analog-to-Digital (A/D) Converters are devices that convert a voltage level from a sensor to a digital word usable by the computer
 - Counting scheme
 - * The input voltage may be converted to a train or pulses whose frequency is proportional to the voltage level.
 - * The pulses are then counted over a fixed period using a binary counter, thus resulting in binary representation of the voltage level.
 - * Counter-based converter might require as many as 2^n cycles.
 - Successive-approximation technique
 - * It is based on successively comparing the input voltage to reference levels representing the various bits in the digital word.
 - * One clock cycle is required to set each bit, so an n -bit converter would require n cycles.
- If more than one channel of data needs to be sampled and converted to digital words, it is usually accomplished using a multiplexer rather than by multiple A/D converters.
- The multiplexer sequentially connects the converter into the channel being sampled.

- Digital-to-Analog (D/A) Converters are used to convert the digital words from the computer to a voltage level and are sometimes referred to as *sample and hold* devices.
 - Because no counting or iteration is required for such converters, they tend to be much faster than A/D converters.
 - A/D converters that use the successive approximation method of conversion include D/A converters as components.
 - The price of D/A converters is comparable to A/D converters, but usually somewhat lower.
- Computer is the device where the compensation $D_d(z)$ is programmed and the calculations are carried out.

- Analog Anti-Alias Prefilters are often placed between the analog sensor and the A/D converter.
 - An example of aliasing is shown Fig. 8.16, where 60Hz oscillatory signal is being sampled at 50Hz. The figure shows the result from the samples as a 10Hz signal and also shows the mechanism by which the frequency of the signal is aliased from 60 to 10Hz.

Figure 8.16

An example of aliasing



- Its function is to reduce the higher frequency noise components in the analog signal in order to prevent *aliasing*.
- Aliasing will occur any time the sample rate is not at least twice as fast as any of the frequencies in the signal being sampled.
- To prevent aliasing of a 60Hz signal, the sample rate would have to be faster than 120Hz.

- Aliasing can be explained from the *sampling theorem* of Nyquist and Shannon. For the signal to be reconstructed from the samples, it must have no frequency component greater than half the sample rate (*Nyquist rate* of $\omega_s/2$).
- In a continuous system, noise components with a frequency much higher than the control-system bandwidth normally have a small effect because the system will not respond at the high frequency.
- However, in a *digital system*, the frequency of the noise can be *aliased down* to the vicinity of the system bandwidth so the closed-loop system would respond to the noise.
- The solution to prevent aliasing is to place an analog prefilter before the sampler. In many cases, a simple first-order low-pass filter will do - that is -

$$H_p(s) = \frac{a}{s + a}$$

where the *breakpoint* a is selected to be lower than Nyquist rate $\omega_s/2$ so that any noise present with frequencies greater than Nyquist rate is attenuated by the prefilter.

- If ω_s is chosen to be $25 \times \omega_{bd}$, the anti-aliasing filter breakpoint a should be selected lower than $\omega_s/2$, so that

$$a = 10 \times \omega_{bd} \quad \leftarrow \quad \omega_s = 25 \times \omega_{bd}$$

would be a reasonable choice.

5 Sample-Rate Selection

- The inherent approximation for the discrete TF may give rise to *decreased performance* or even *system instability* as the sample rate is lowered. This can lead the designer to conclude that a faster sample rate is required.
- The *sampling theorem* states that in order to reconstruct an unknown, band-limited, continuous signal from samples of that signal, we must *sample at least twice as fast as the highest frequency contained in the signal*. $\omega_s = 2\omega_{bd}$
- In the z -plane, the highest frequency that can be represented by a discrete system is $\omega_s/2$.
- For a very high frequency noise, it would be foolish to sample fast enough to attenuate the disturbance without the use of a prefilter.

6 Discrete Design

- This plant model can be used as part of a discrete model of the feedback system including the compensation $D_d(z)$.
- Analysis and design using this discrete model is called *discrete design* or alternatively, *direct digital design*.
- For a plant described by $G(s)$ and preceded by a ZOH, the discrete TF was essentially given by

$$G(z) = (1 - z^{-1})\mathcal{Z} \left\{ \frac{G(s)}{s} \right\}$$

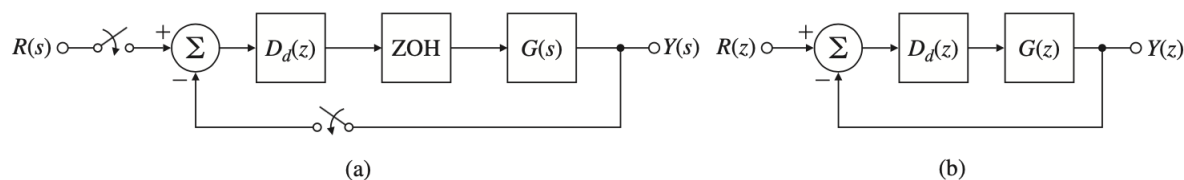


Figure 8.17

Comparison of: (a) a mixed system; and (b) its pure discrete equivalent

- The closed-loop poles or the roots of the discrete characteristic equation

$$1 + D_d(z)G(z) = 0$$

- The root-locus techniques used in continuous systems to find roots of a polynomial in s apply equally well and without modification to the polynomial in z .
- The interpretation of the results is that the stability boundary is now the unit circle instead of the imaginary axis.

(Example 8.4) When $G(s) = \frac{a}{s+a}$ and $D_d(z) = K$, draw the root locus with respect to K ?
 (Answer)

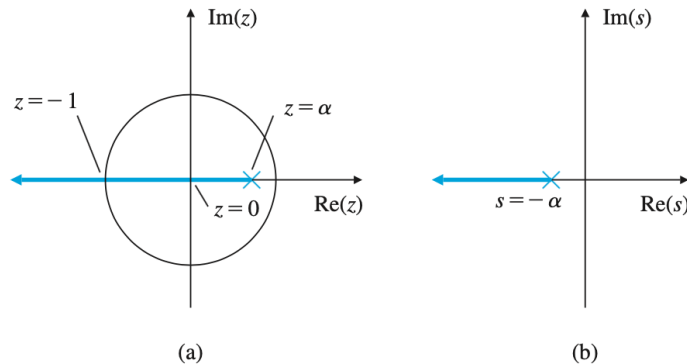
$$\begin{aligned}
 G(z) &= (1 - z^{-1}) \mathcal{Z} \left\{ \frac{a}{s(s+a)} \right\} = (1 - z^{-1}) \mathcal{Z} \left\{ \frac{1}{s} - \frac{1}{s+a} \right\} \\
 &= (1 - z^{-1}) \left(\frac{1}{1 - z^{-1}} - \frac{1}{1 - e^{-aT} z^{-1}} \right) \\
 &= \frac{(1 - e^{-aT}) z^{-1}}{1 - e^{-aT} z^{-1}} \\
 &= \frac{(1 - \alpha) z^{-1}}{1 - \alpha z^{-1}} \quad \text{where } \alpha = e^{-aT}
 \end{aligned}$$

The discrete characteristic equation becomes

$$1 + D_d(z)G(z) = 1 + K \frac{(1 - \alpha) z^{-1}}{1 - \alpha z^{-1}} = 0$$

Figure 8.18

Root loci for: (a) the z-plane; and (b) the s-plane



In the continuous case, the system remains stable for all values of K . In the discrete case, the system becomes oscillatory with decreasing damping ratio as z goes from 0 to -1 and eventually becomes unstable. This instability is due to the lagging effect of the ZOH.

Feedback properties

- Proportional

$$u(k) = Ke(k) \quad \leftrightarrow \quad D_d(z) = K$$

- Derivative

$$u(k) = KT_D[e(k) - e(k-1)] \quad \leftrightarrow \quad D_d(z) = KT_D(1 - z^{-1})$$

- Integral

$$u(k) = u(k-1) + \frac{K}{T_I}e(k) \quad \leftrightarrow \quad D_d(z) = \frac{K}{T_I} \left(\frac{1}{1 - z^{-1}} \right)$$

- Lead

$$u(k) = \beta u(k-1) + K[e(k) - \alpha e(k-1)] \quad \leftrightarrow \quad D_d(z) = K \frac{1 - \alpha z^{-1}}{1 - \beta z^{-1}}$$

(Example 8.5) Design a digital controller to have a closed-loop natural frequency $\omega_n = 0.3$ and a damping ratio $\zeta = 0.7$ using discrete design

(Answer)

$$G(s) = \frac{1}{s^2} \quad \rightarrow \quad G(z) = (1 - z^{-1})\mathcal{Z} \left\{ \frac{1}{s^3} \right\} = \frac{T^2 z^{-1}(1 + z^{-1})}{2(1 - z^{-1})^2}$$

which, with $T = 1$, becomes

$$G(z) = \frac{1}{2} \frac{z^{-1}(1 + z^{-1})}{(1 - z^{-1})^2}$$

Let us assume that the PD compensator is used

$$D_d(z) = K(1 - \alpha z^{-1})$$

The desired pole locations of $\omega_n = 0.3$ and $\zeta = 0.7$ become $z = 0.78 \pm 0.18j$

$$1 + D_d(z)G(z) = 1 + K \frac{1}{2} \frac{z^{-1}(1 + z^{-1})(1 - \alpha z^{-1})}{(1 - z^{-1})^2} = 0$$

Now we have

$$\alpha = 0.85 \quad K = 0.374$$

and

$$D_d(z) = 0.374(1 - 0.85z^{-1})$$

The difference equation becomes

$$u(k) = 0.374[e(k) - 0.85e(k - 1)]$$

(8장 숙제) 15개의 문제 중 4개 풀어 제출